PCBs Practice 5:

Final Report

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# Introduction

The following document contains the final report 4 for PCBs.

In this document is intended to be used for future references, so this document contains how to, problematic found during the development of the practices, best practices and hints.

Thought this document it will be described the whole procedure to create a PCB with Allegro 16.3 version. The following applications are involved in this process:

1. PCBM LP Calculator
2. Pad Designer
3. Allegro Design Entry CIS
4. PCB Editor XL
5. Placement Constrains manager (DFA)
6. Physical/Electrical/Spacing Constrains manager (CM)

Through this document it will be explained the whole process to create a PCB.

# High Level overview of steps involved in PCBs for Gerbers creation

The following describes the sequence to create PCB:

1. **Library creation.** Consists of creating the logical drawings that represents the parts, these logical drawings will be used in the creation of the schematics.
2. **Pad Stack Creation**. Consists of creating the pad stack, that is, the base areas where the parts will be soldered.
3. **Footprint Creation**. Consists of creating the physical drawing of the parts, these physical drawings will be used for the creation of the layout.
4. **Schematic Creation**. Consists of creating a drawing of the whole parts and connections between them. This is a logical picture of the board/circuit.
5. **Layout Creation**. Consists of creating a drawing of the whole parts and connection between them. This is a physical picture of the board/circuit.
6. **Gerber Creation**. Consists of creating the manufacturing files for the board.

# High Level overview of tools involved

The following are the list of tools involved in the process of PCBs:

1. **PCBM LP Calculator**

This is a freeware tool used to calculate lengths for required for pad stacks

1. **Pad Designer**

Through this tool the pad stacks required for foot prints are created.

1. **Allegro Design Entry CIS**

Through this tool the following are created:

1. Libraries
2. Schematics.
3. **PCB Editor XL**

Through this tool the following are created:

1. Footprints
2. Board
3. Layout
4. Gerbers
5. **Placement Constrains manager (DFA)**

Through this tool the Placement constrains are created.

1. **Physical/Electrical/Spacing Constrains manager (CM)**

Through this tool the constrains required for routing are created.

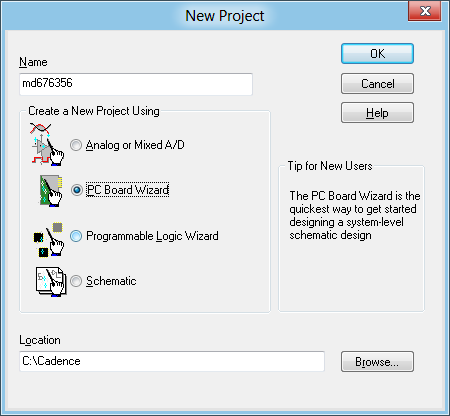
The rest of this document is an abstract of several parts of previous practices which will provide a full picture of the PCBs.

# Creating a project for libraries/schematics

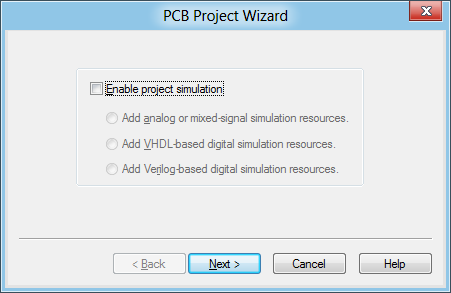
The following section describes the initial step to create an ORCAD project for a PC Board:

1. Open ORCAD Capture CIS
2. Go to File\New\Project
3. Fill information on **"New project"** and press "OK" button:

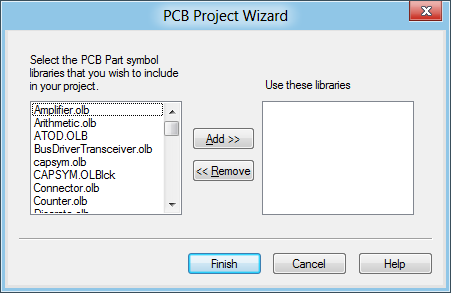
In this dialog you will indicate the type of project, location and name.



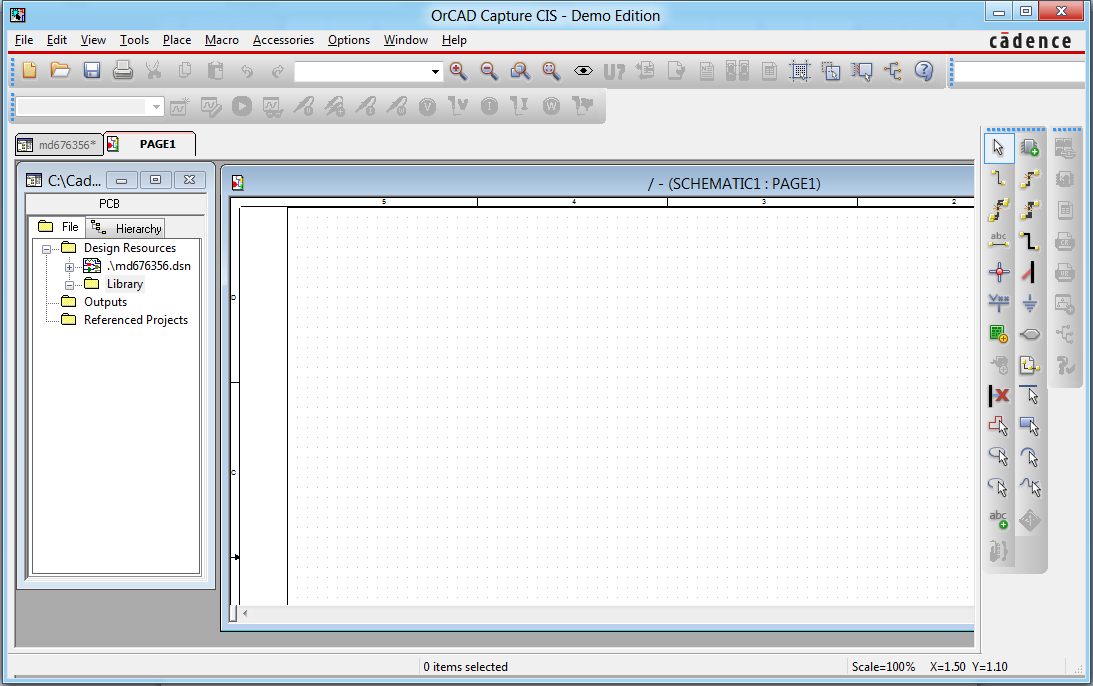
1. Indicate if project simulation will be required:
   1. leave **"enable project simulation"** unchecked
   2. Press **"Next"** button.



1. select the list of libraries to be used in your project:
   1. for our the practice 1 purposes, no libraries will be required to be added
   2. Press **"Finish"** button.



1. The Orcad capture CIS project is ready to work with it:



# Creating Library structure

One created the project the next step is to create the libraries structure for the project...

In this step it is important to create as many as required libraries and sub libraries in order to make easier to reference and locate them when required later.

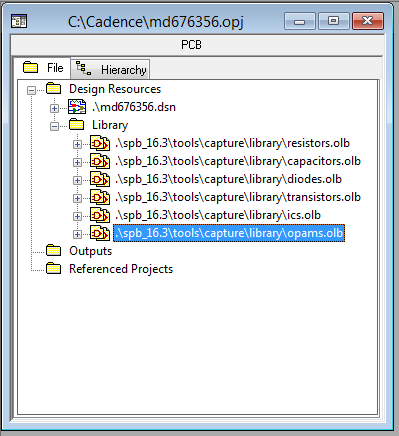
As an example, the following is an alternative to organize them:

* Resistor
* Capacitors
* Diodes
* Transistors
* ICs
* OPAms

Additional, sublibraries may be created on them if libraries will contain lot of parts.

The following are the steps to create the libraries structure

1. Select library folder
2. Go to File\New\Library
3. Doing this a library1.olb will be added below the library folder.
4. Rename it to the proper name by:
   * Right clicking on it
   * select **"Save as"**
   * update the library with the new name and press **"Save"** button.
5. Repeat steps 1 - 4 until completed the libraries structure.



# Adding a part manually into libraries

One created the library structure the next steps is to add parts to the libraries...

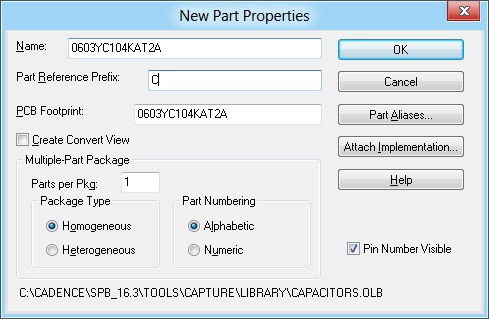
There are a couple of different ways to create parts, this section will explain the long way to create parts which is more useful for simple parts. For complex parts like ICs with lot of PINs it is recommended to use spreadsheet method to speed up the creation and maintenance.

The following steps show how to add the part:

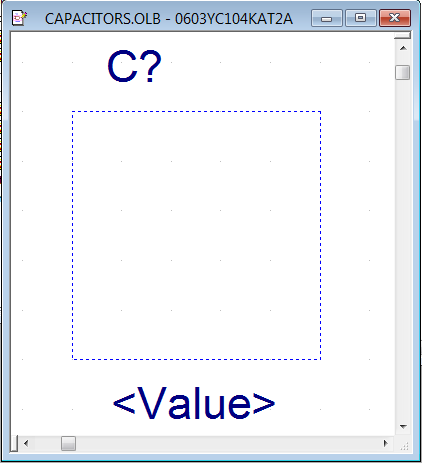
1. Select the library where the part will be added
2. Right click on it
3. Select New Part and fill Dialog information as follow:

* Name ==> Part name.
* Prefix ==> Identifier for the part:
  + C ==> Capacitor
  + R ==> Resistor
  + U ==> unit .....
* PCB footprint ==> PCB footprint

The following screen shows how to enter information about a new capacitor:



By pressing "**OK"** button the following screen will be created:



Where:

**C?** ==>

C ==> Capacitor

? ==> Capacitor Name which will be replaced by a consecutive number automatically at the time to create the schematic.

**Value** ==> Capacitor value, you can specify here all details you want.

**Note**: is it important to define a naming standard for the description of this part.

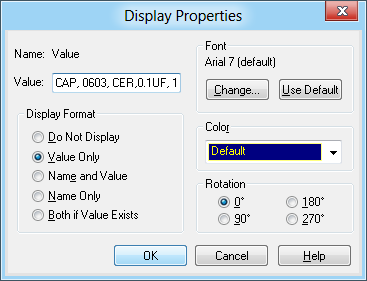
**Dotted square** ==> Area representing the symbol (at this point there are not symbol defined yet. See creating the part symbols for more details how to do this).

4. In order to add the capacitor name do the following:

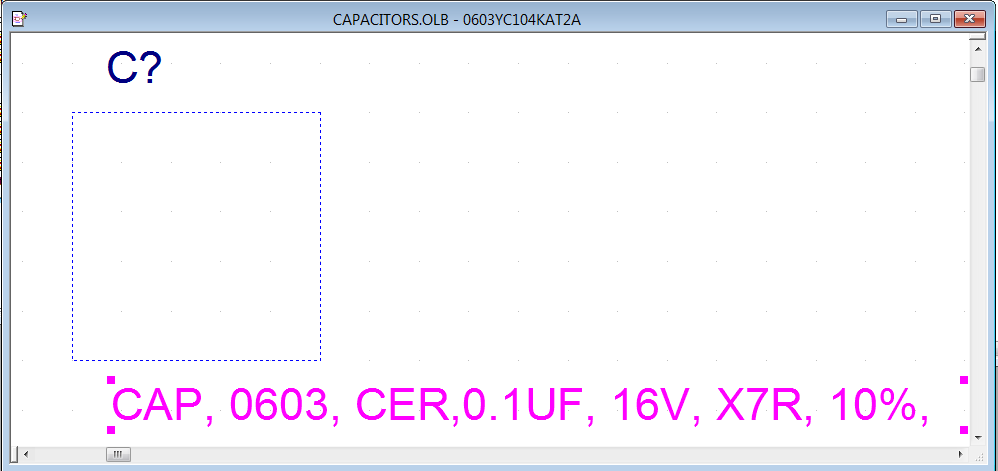
- Right click on Value

- Select **"edit properties"** option

- fill the part’s value:



- By pressing "**ok**" button it will update the value name as follow:



# Creating the part symbol in libraries

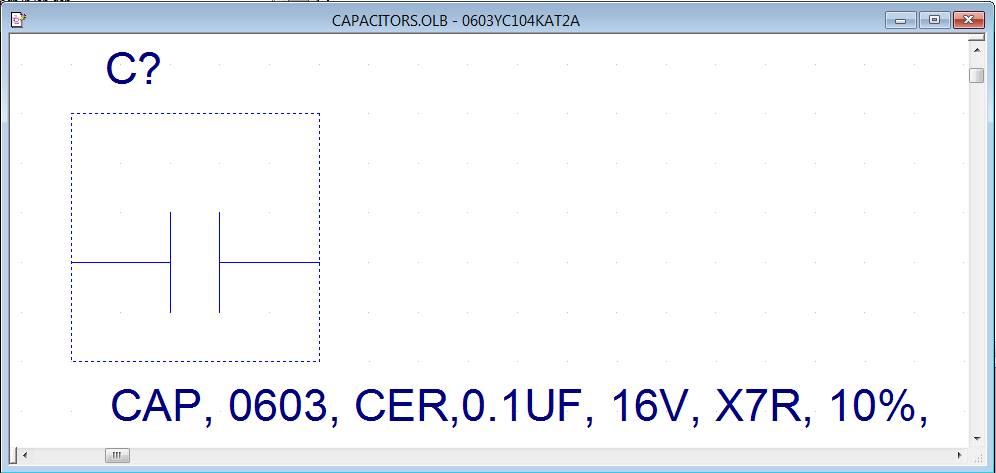
At this point the part was already created but has not symbol yet.

The Draw menu displayed bellow will be used to create the symbol:



For instance, to create symbols follow these steps:

1. Click on the Place liner icon ()
2. Draw the symbol. See following picture:



3. Press **"CTL+S"** or go to "**File\Save**" to save the project.

# Adding pins to the symbol in libraries

In order to add a pin number do the following:

1. Click on the pin number icon ()
2. In the dialog box opened
   1. Fill the pin name field.

Note:

If it is a part asserted in zero, put backslash before each letter. Example:

Name field = VCC 🡺 Pin name = VCC

Name field = \R\E\S\E\T 🡺 Pin name =RESET

* 1. Fill the pin number.

Note:

Pin number must be unique in a part.

# Creating the footprints (Opening the Specs)

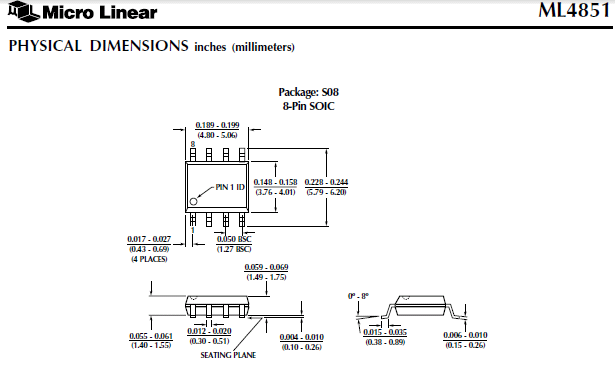
The links to the specs are contained in the excel sheet with the list of BOMs.



This link row contains the link to the following link to the specs:

<http://www.datasheetcatalog.org/datasheet/MicroLinearCorporation/mXyzrwuw.pdf>

Locate on the spec the part where it contains the chip dimensions see following figure:



# Calculating Pad Stacks sizes for footprints

PCBM LP Calculator helps to calculate the pad stack sizes based on the dimensions provides by the Specs for a SOIC 8.

The following procedure shows how to do that step by step:

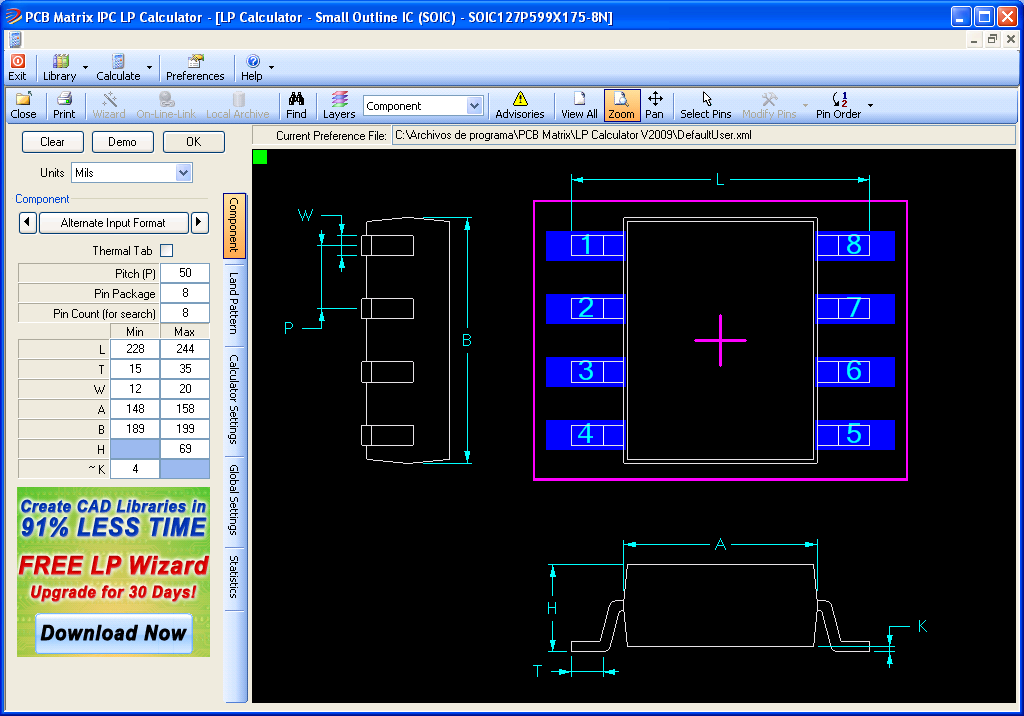
1. Open “PCBM LP Calculator”
2. Click on “Calculate” Icon 
3. Select “SMD Calculator” 
4. Select “Small Outline IC (SOIC):
5. This will create a new dialog showing an IC with 20 pins. **It does not matter the numbers of PINs At this point, the picture with the proper number of pins will be updated later.**
6. Select the units you want, It is recommended to select mills or millimeters in this case Mills will be used: 
7. Fill the values in the Calculator based on the specs.

**Notes:**

1. The letters in the calculator doesn’t match the letters on the specs, so check the dimensions instead of letters in the calculator.
2. In the specs the measures are in inches but in this part they will be introduced as mils. Example:

0.228 inches 🡺 244 mils

1. Press OK button to draw the proper chipset 



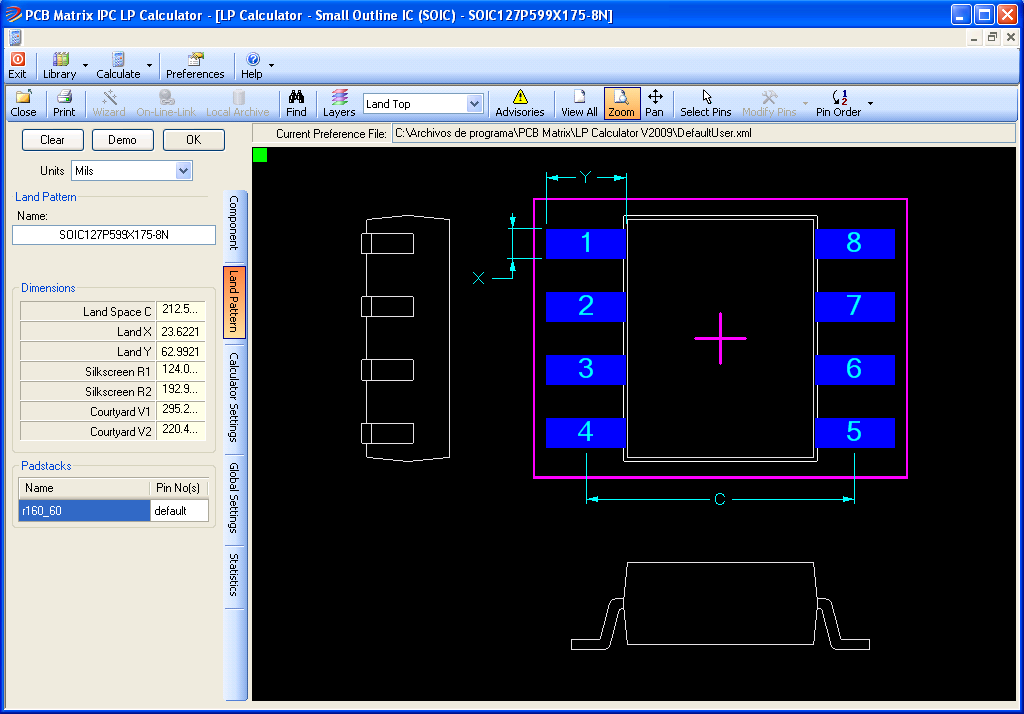
1. Click on Land Pattern tab to display the calculated **Land X** and **Land Y** which will be used later to create the pad stacks **.**

The values must be rounded up ex:

**Land X = 23.6221 🡺 24**

**Land Y = 62.9921 🡺 63**

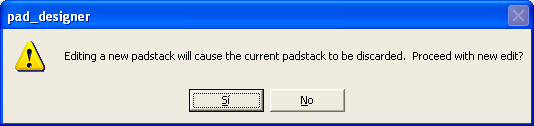
See following picture:



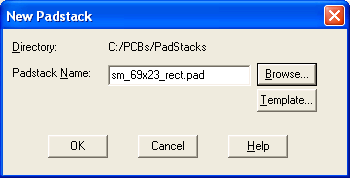
# Creating the pad stacks for footprints

Once calculated the Land X (24 mils) and Land Y (69 mils) values is time to create the pad stacks so do the following:

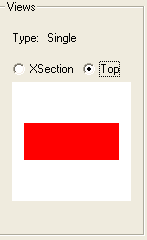
1. Open Pad Designer:
   1. 
   2. 
   3. 
   4. 
2. Create the Pad Stack name:
   1. Go to File\New
   2. Press “ok” (“Si”) to create the new pad stack:



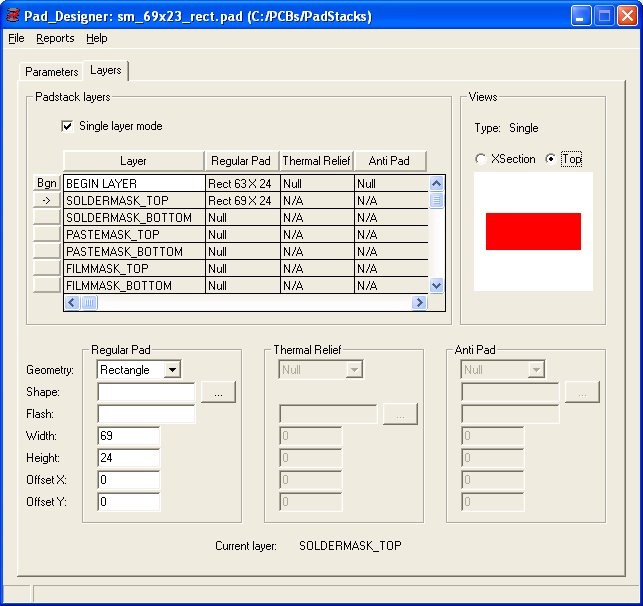
* 1. If no already created, create a subdirectory to store all pad stacks: 
  2. Standards must be used for pad stacks naming as follow:
     1. sm 🡺 surface mount
     2. 63x24 🡺 LandX x LandY
     3. Rect 🡺 Type of pad stack
  3. Press “Open”/”Abrir” button 
  4. Press “Ok” button on the following dialog box

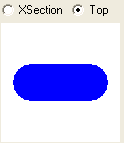


1. On parameters tab () Select mils as the current units 
2. On **Layers** tab () check “Single Layer Mode” Checkbox 
3. Select the geometry for the padstack of the PIN 1 
4. **Notes:**
   1. Following the standards for PCBs and to distinguish pin 1 from the rest of the pins:
      1. Rect padstack type will be used for pin 1
      2. Oblong padstack type will be used for the rest of the pins.
5. Fill the BEGIN LAYER and SOLDERMASK\_TOP

* **Notes:**
  + Width 🡺 Land X 🡺 63
  + Height 🡺 Land Y 🡺 24
  + For SOLDERMASK\_TOP With must be increased by 6, that is, 69.
  + On views you can select the type of view Example: 

The following picture showing the values introduced:

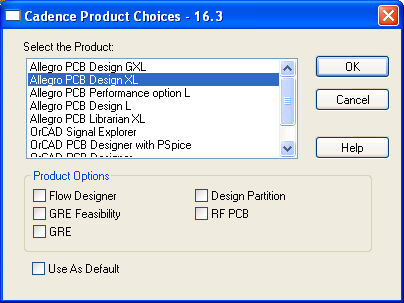


1. At this point the pad stack for PIN 1 was created. So let’s create the pad stack for the rest of the PINs, which is done as follow:
   1. Go to “File” menu on “Save as” option.
   2. Save it as sm\_69x23\_oblong.
   3. Select Geometry as oblong: 
   4. Check view changed to oblong 
   5. Save padStack again through File menu and Save option
   6. Press OK to overwrite existing padstack.

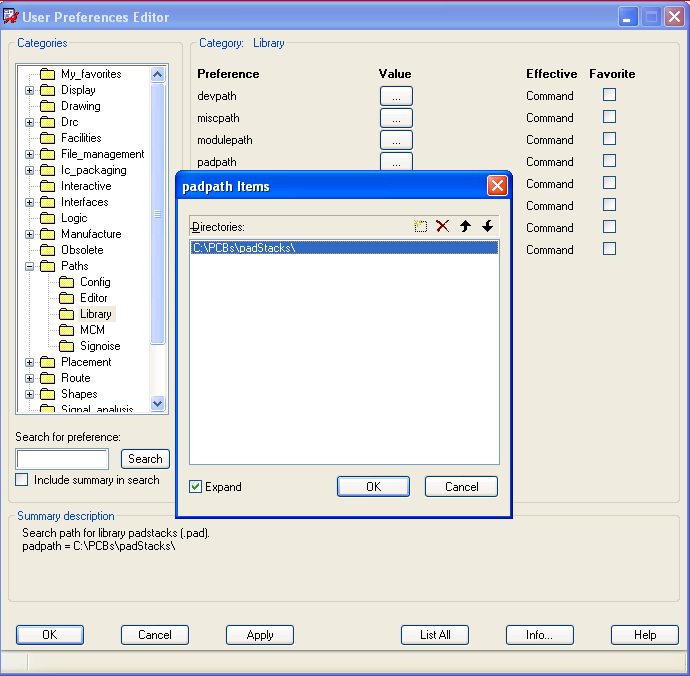
# Creating the footprint

Once the Padstacks are created it is time to create the footprints. In order to create the footprints do the following:

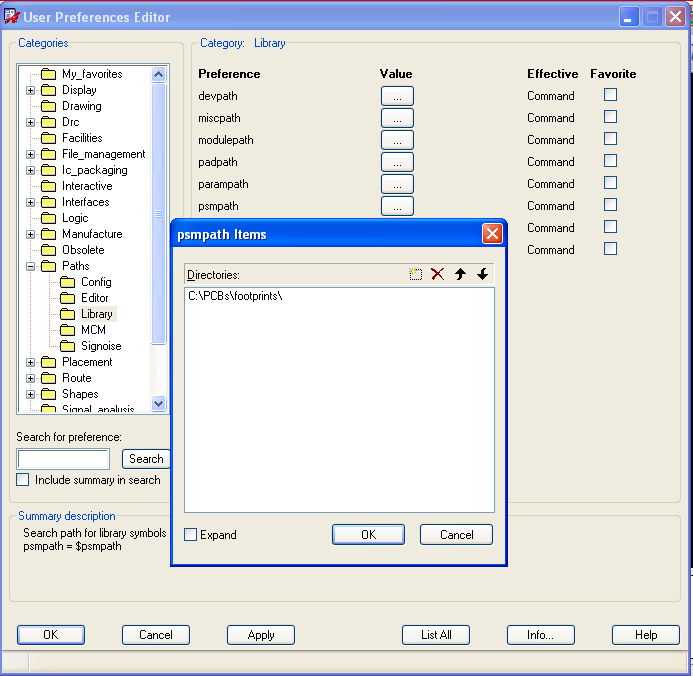
1. Open PCB Editor:
   1. 
   2. 
   3. 
2. Select the Allegro PCB Design XL option:



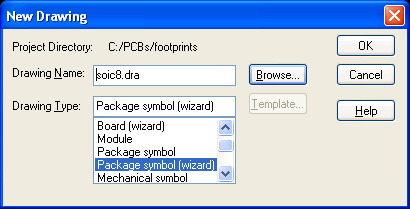
1. Configure the paths for the PadStacks and footprints as follow:
   1. On **Setup** menu **Preferences** option..
   2. Expand **Paths**
   3. Click on **Library**
   4. Click on **PadPath**
   5. Update the path where the PadStacks were located. See following picture:



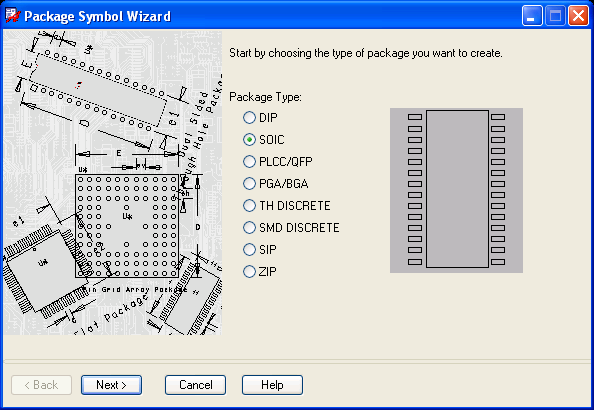
* 1. Update the footprints directory also by clicking on psmpath:



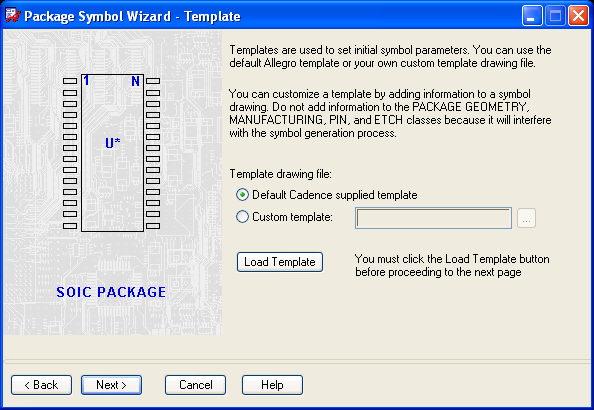
1. The following steps will show you how to create the part using the Wizard:
   1. Go to **file** menu, on **New** option:
   2. Fill the name of the package and select **Package Symbol (Wizard)**:



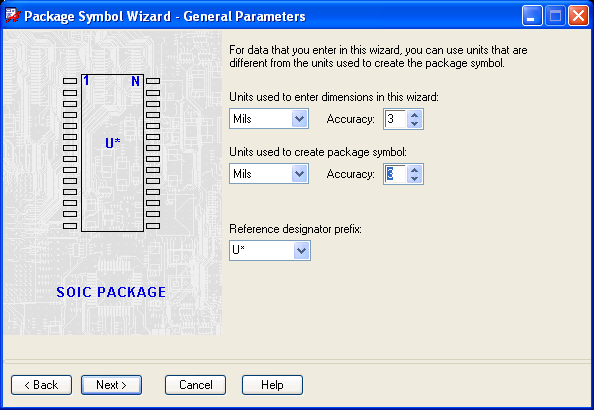
* 1. Select **SOIC** radio button and press **Next** button:



* 1. Load the default template () this will load a grid which corresponds with the template just loaded:



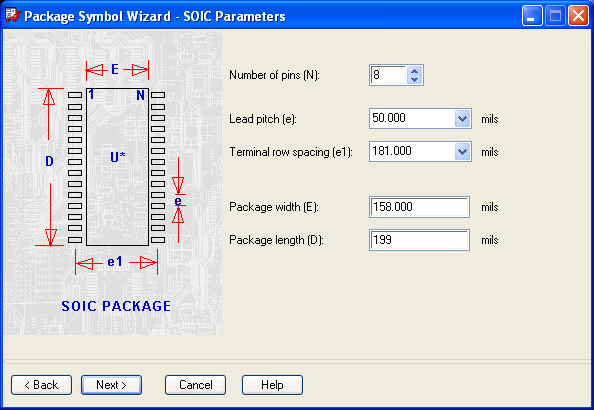
* 1. Press **Next** button
  2. Fill the Accuracy and Reference designator prefix and press **Next** button.



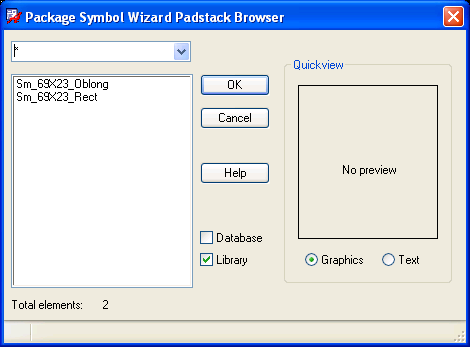
* 1. Fill the measures based on the data from the PCB calculator:

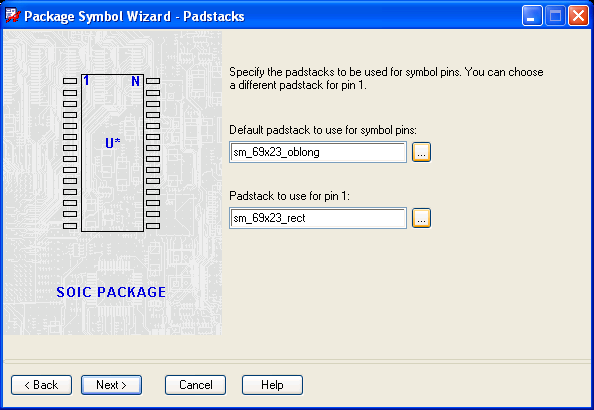
**Notes:**

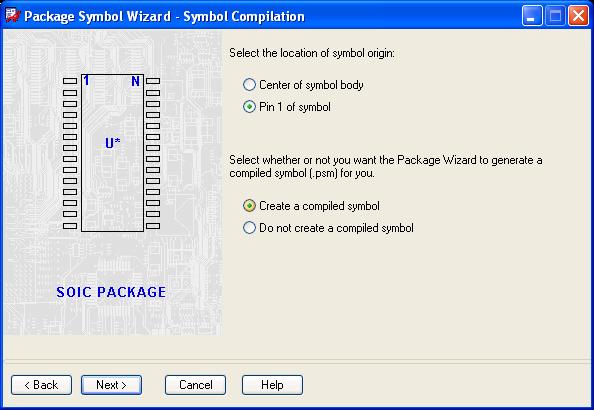
* + 1. Terminal Row spacing (e1) is calculated as follow:
* E1 = L - 63 🡺 244 – 63 🡺 181



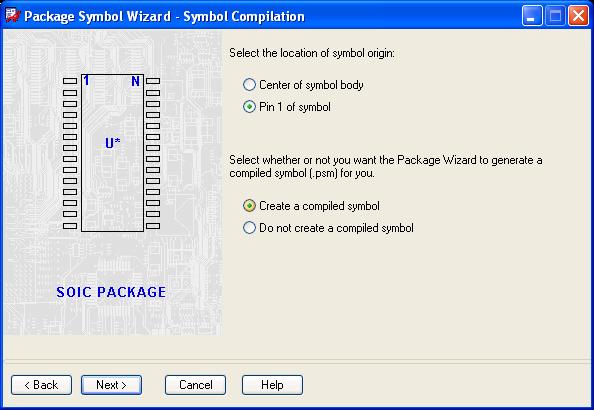
* 1. Load the PadStacks previously created:



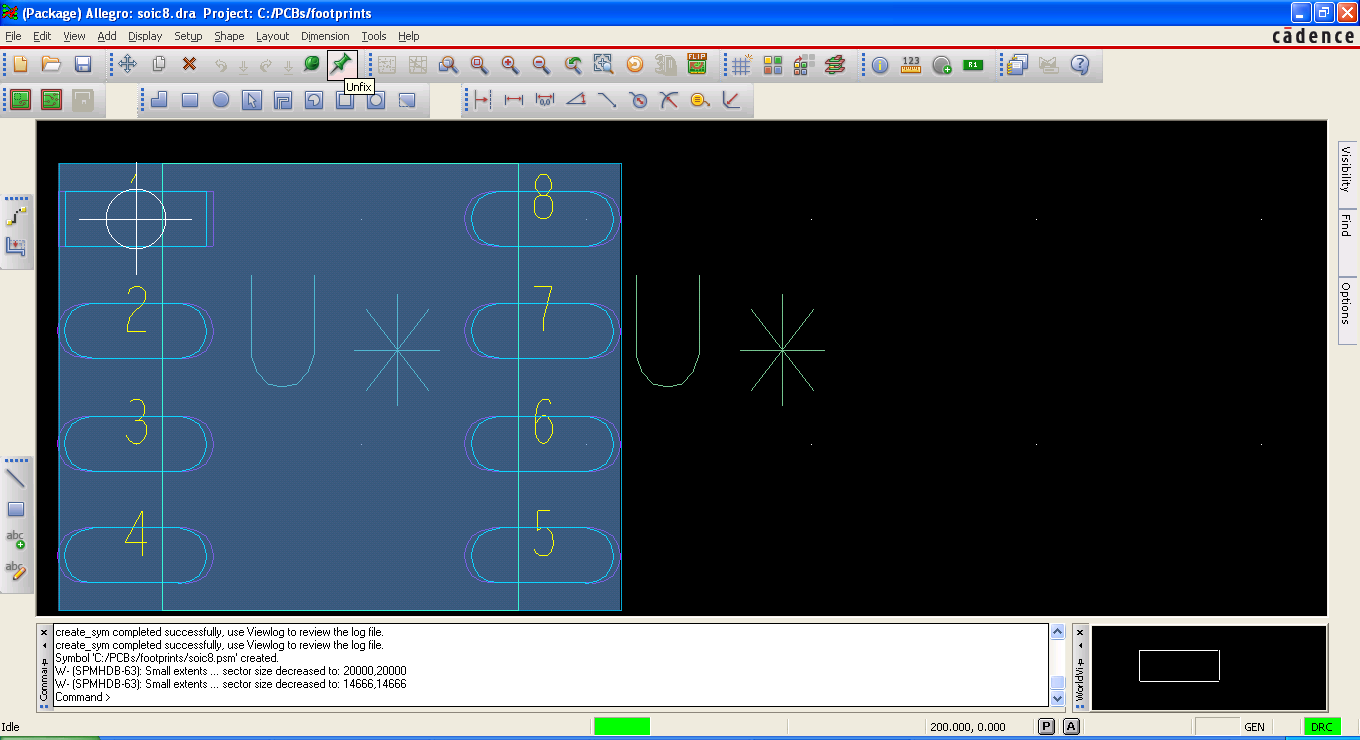




Press finish to complete the Package Symbol:



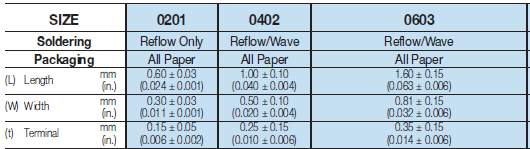
This will create the package symbols as follow:

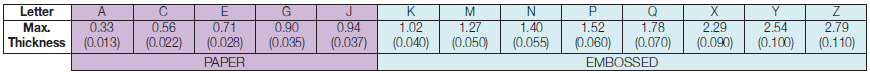


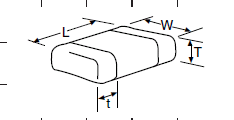
# Creating footprints for capacitors/resistances

Due to the process to create footprints for capacitors and resistors is a little different, this document describes in a faster what how to do it:

1. Open the Specs and locate the dimensions and shape:







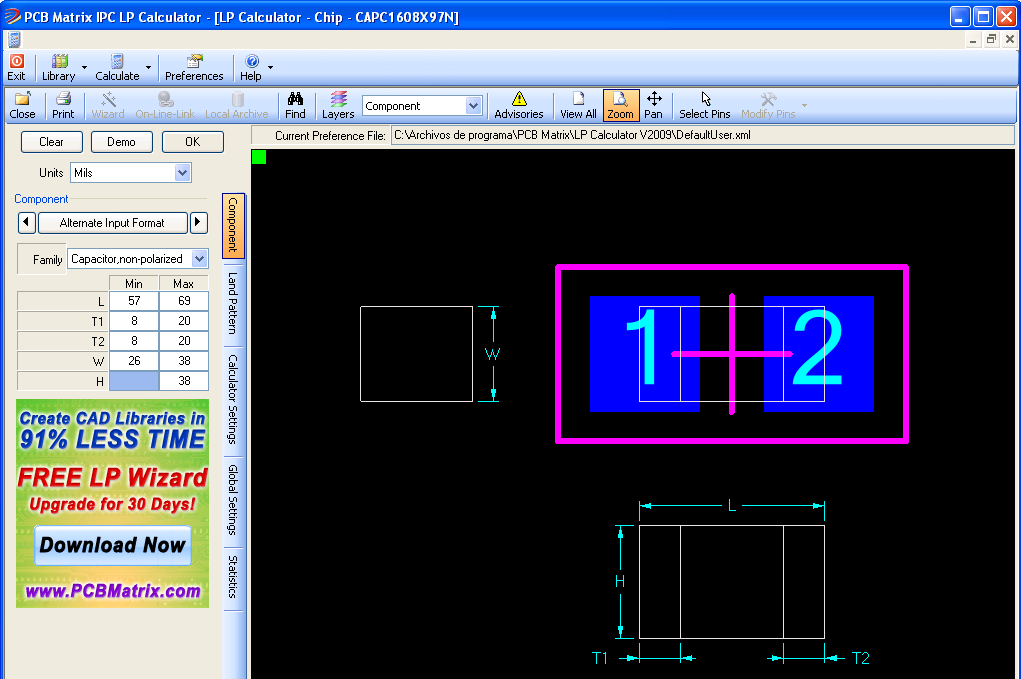
Notes:

1. For capacitors and resistors the measures has some tolerance, so the value to introduce must consider that tolerance.

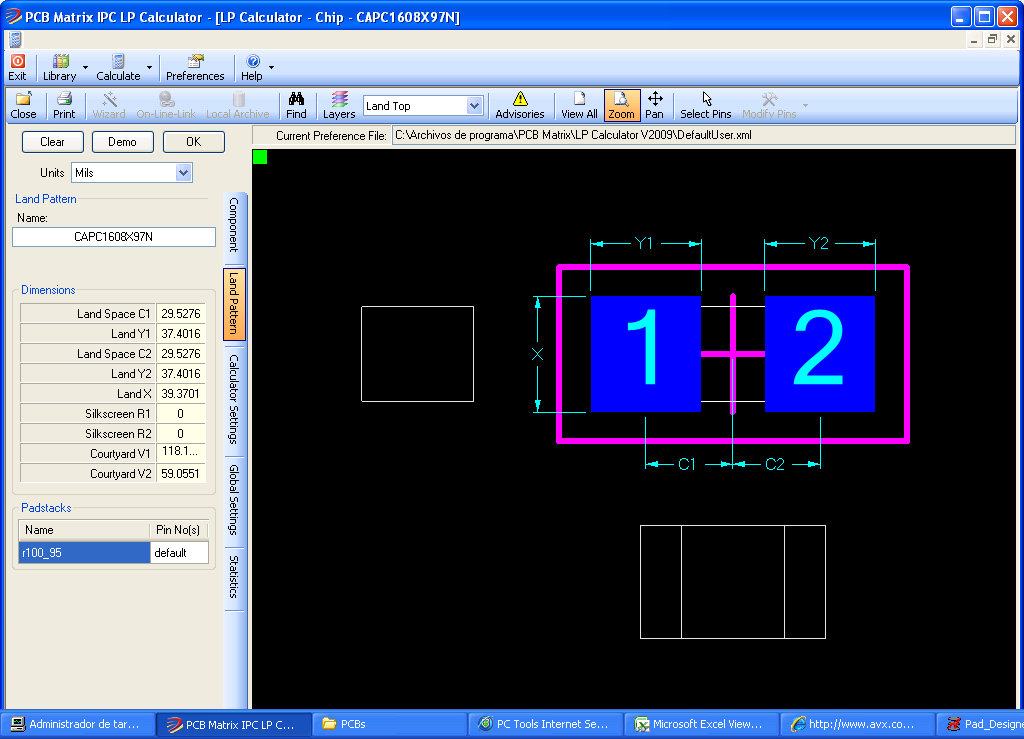
For instance: measure for 0603 in mils:

* 1. L 🡺 0.063 +- 0.006
  2. So values to be introduced in PCB Calculator must be MIN=57 and MAX=69

1. Fill the values in the calculator as showed in the following picture:



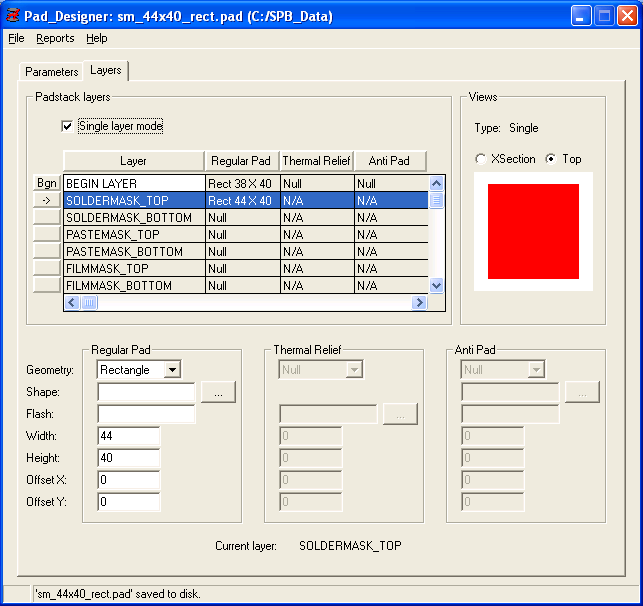
1. Press **OK** button and Select **Land Pattern** tab to obtain the Land X and Land Y1:



1. Now launch **Pad designer** and fill the values.

**Notes:**

* + Both pad Stacks will be created (**Land X, Land Y1 and Land Y2**)
  + Land Y1 and land Y2 has the same value
  + Remember to round up the values
  + Remember to check the **Single Layer Mode** checkbox.
  + Remember to add 6 mils to the Width value

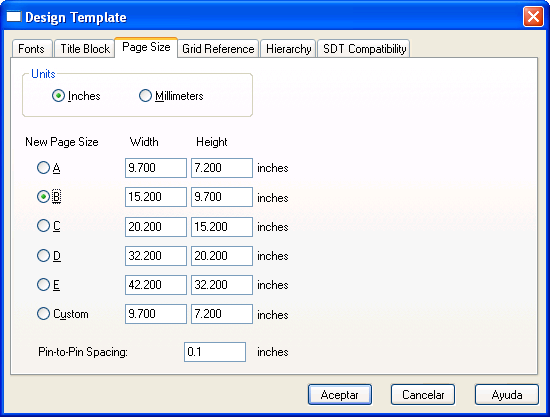


# Creating a blank page for schematic capturing

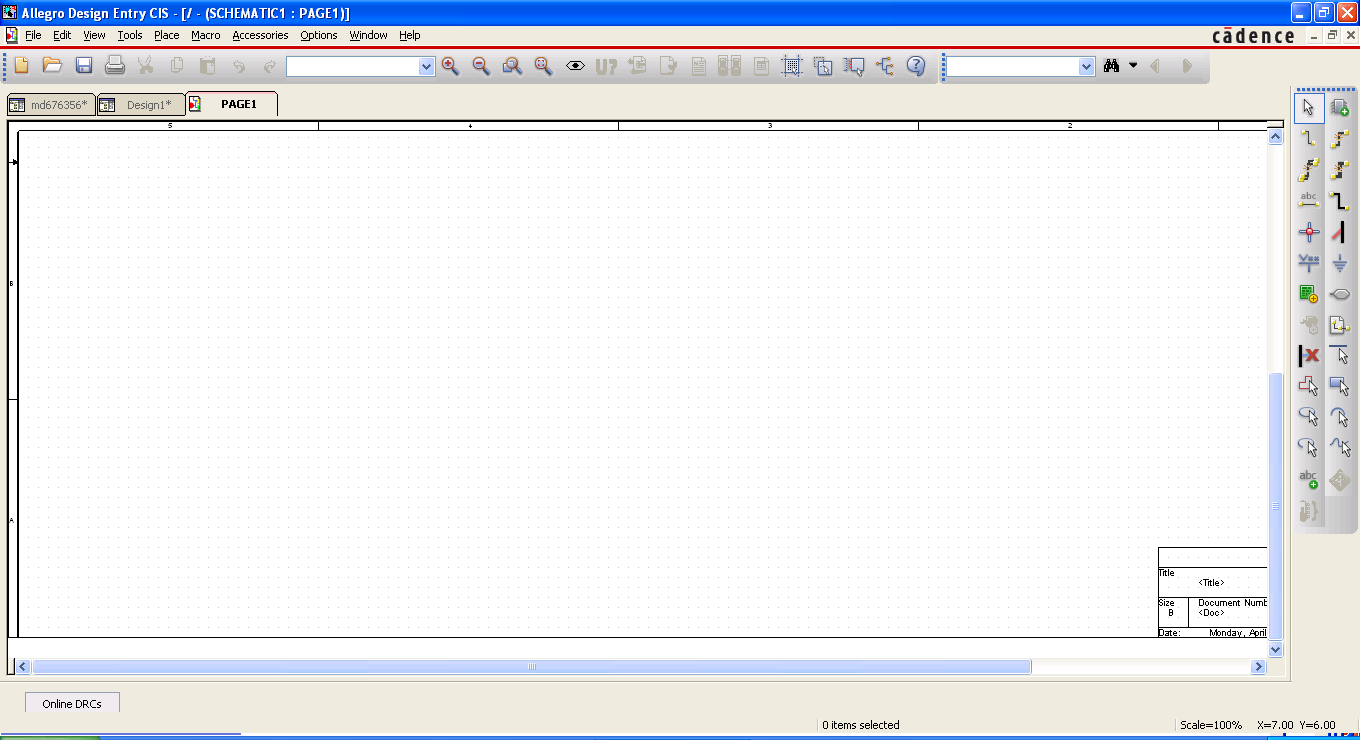
The following procedure shows step by step how to create a blank page for schematic capturing:

1. Open “Allegro Design Entry CIS”
2. Configure the page size as follow:

* Go to “Options”\”Design template” options
* Select “Page Size” tab
* Check the page size:



1. Create a blank design page as follow:
   1. Got to “File”\”New”\”Design” option:



* 1. Review the page size to be the correct one in the bottom right corner.

# Adding parts to the schematic

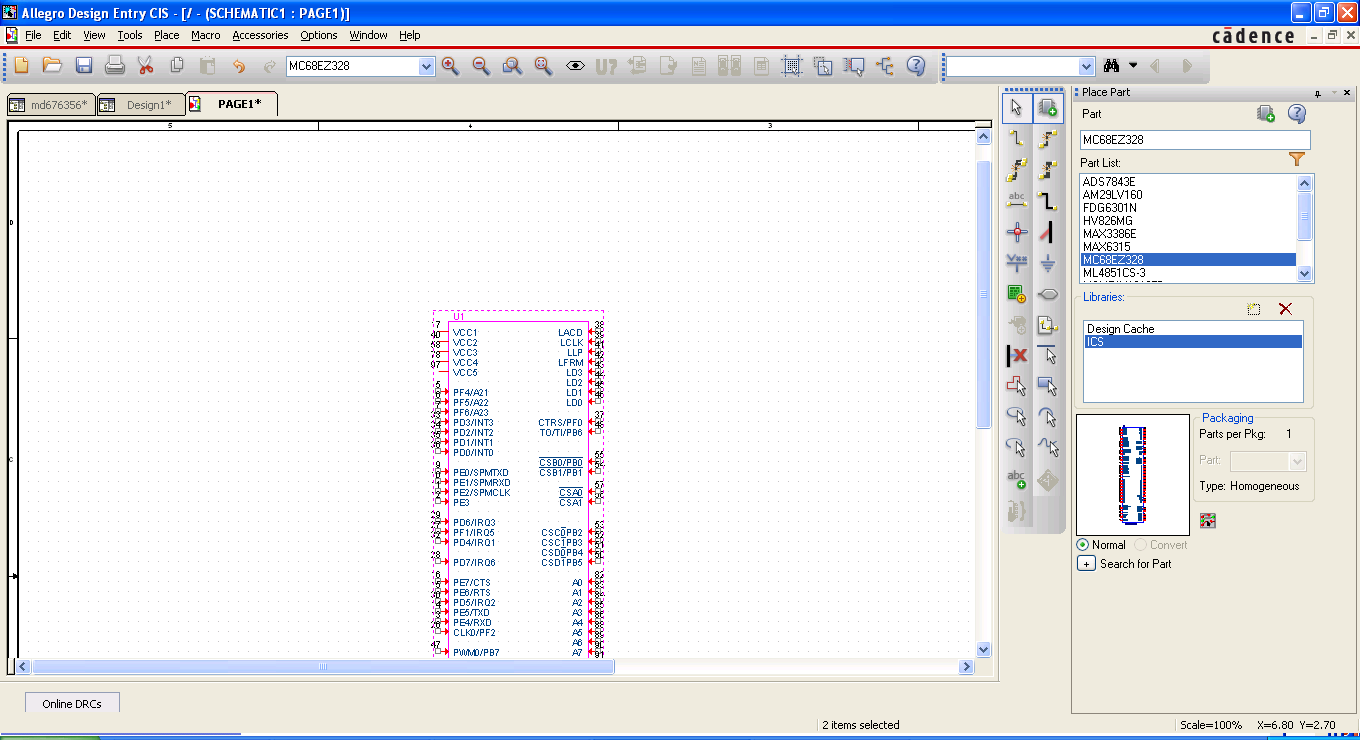
You could place components in any page and any place, however is it recommended to group parts as they will be in the physical layout.

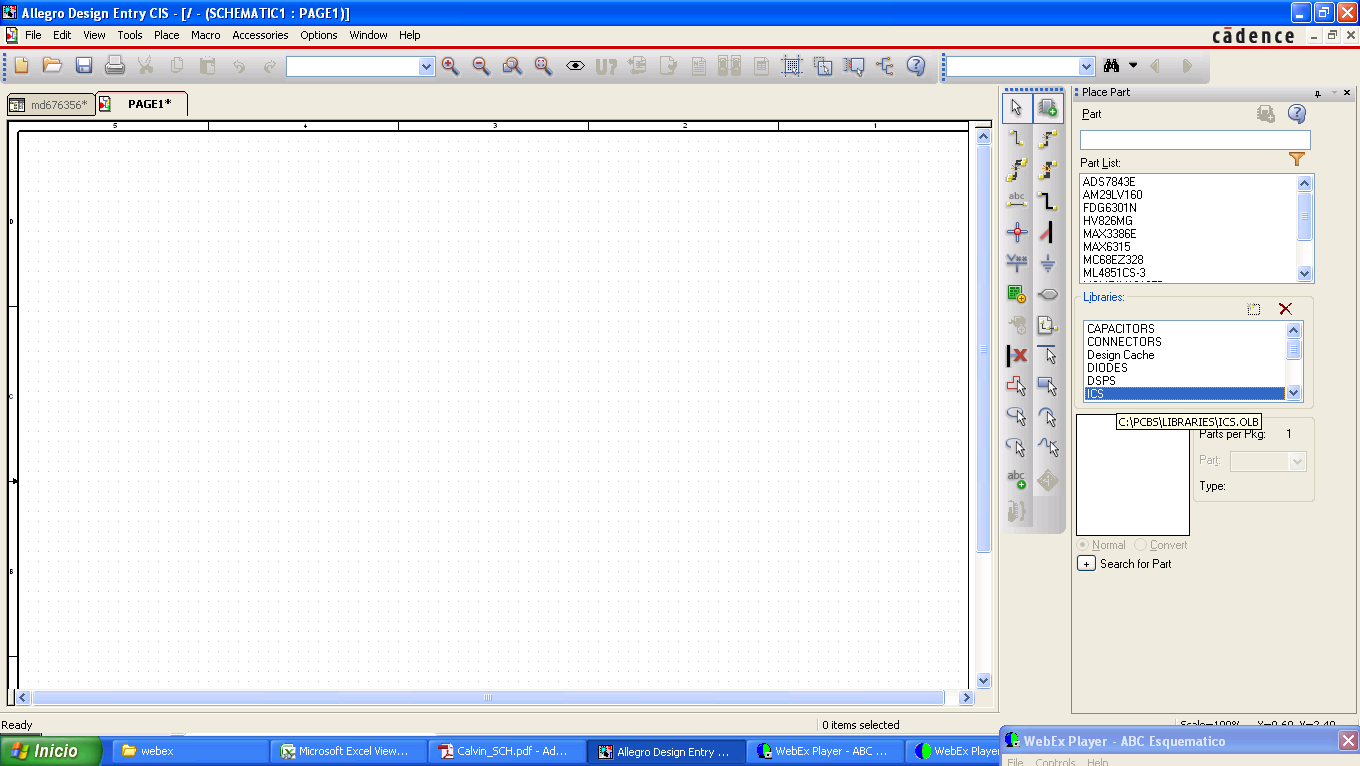
There are no limitations about the number of parts to place in a single schematic

The first step to create a schematic is to add a part. The following will provide some basic guidance about usage of schematic.

1.  🡺 Add a part (from libraries created in practice 1).
2. Open the libraries containing the symbols
3. Double click on the symbol to add
4. Click on the place where the symbol will be placed
5. Right click to display popup menu and select “end mode” option or press ESC key to finish placing the same part.

See following picture:

1. 



1. press OK to overwrite existing padstack.

# Updating parts from cache in to schematic

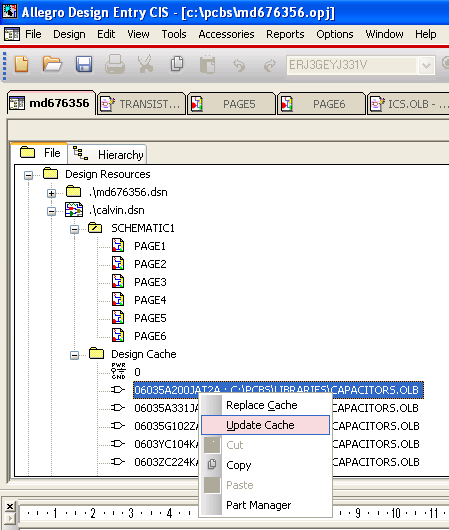
When a part has some error the schematic will show a warning or an error at compilation time. So it is required the following:

1. Fix the issue of the part in the library
2. Update the part already included in the schematic from cache
3. Compile again.

Once the issue is fixed on the library, the cache of the schematic must be updated following these steps:

1. Select the main tab
2. Expand the main design option (\*.dsn field):
3. Expand the Design cache option
4. Right click on the part changed
5. Select “Update Cache”
6. Recompile schematic

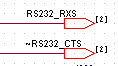
The following screen shot shows how to do this.



# Arrow ports and off page connectors in schematic

There are two groups of connectors between pages:

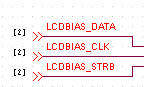
* **Arrow port connectors** 🡺 this kind of symbol is placed when it is the supplier of the signal.



In this case it contains a signal name and a pointing address to inform the type of signal (input, output, bidirectional, power, and etcetera).

The arrow port connectors are followed of an informational text in brackets informing the page or pages where the signal will be send.

* **Off page connectors**🡺 this type of symbol is places when it is the received of a signal generated in some other place (where it is an arrow port connector).



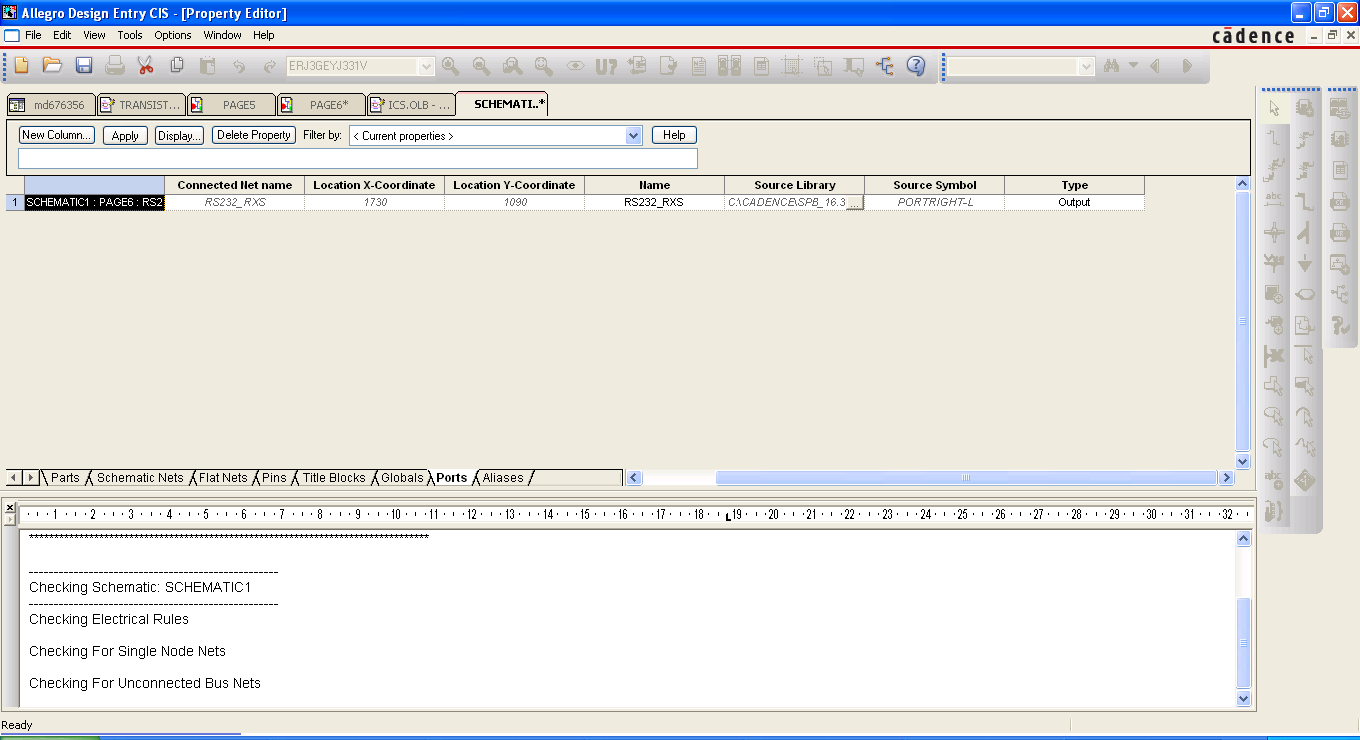
Users cannot change the type of port because it was already defined in another page as an arrow port connector.

The off page connectors are followed of an informational text in brackets informing the page or pages where the signal was generated.

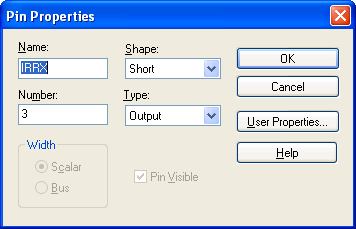
Arrows port symbols are confusion because it can have an entrant orientation but it currently is an output port. So it is required to check what is the current meaning for it and don’t assume the orientation is correct. On the other hand, it is recommended to have a symbol orientation that visually represents whether it is output or input.

At compilation time there will be several errors indicating input ports connected to output pins and vice versa, in order to fix this problem you need to update the port symbol or update the type of pin. The following is the procedures to update these.

**Updating the port type of the symbol**

1. Double click on the arrow port connector in the schematic. It will show the following screen.
2. Update the port Type (ie. Output to input)
3. Close the tab.

**Updating the pin type**

1. Open the part in the library
2. Double click on the pin to be updated. It will display the following screen.
3. Fix the pin information
4. Save the part
5. Update schematic cache
6. Recompile schematic

# More icons to create schematics

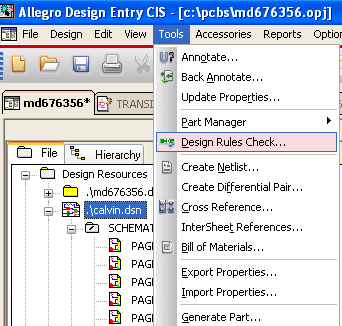
The following shows the list of icons and their function

*  selection mode
*  Single point Net connection
*  Multiple points Net connection
*  Net aliases
*  Put explicit connection where lines crossed
*  VCC symbols
*  GND symbols
*  Hierarchical block
*  No connect
*  Single bus connection
*  Multibus connection
*  bus
*  bus entry
*  arrow ports connectors
*  off page connectors
*  symbols to draw informational figures only
*  informational text.

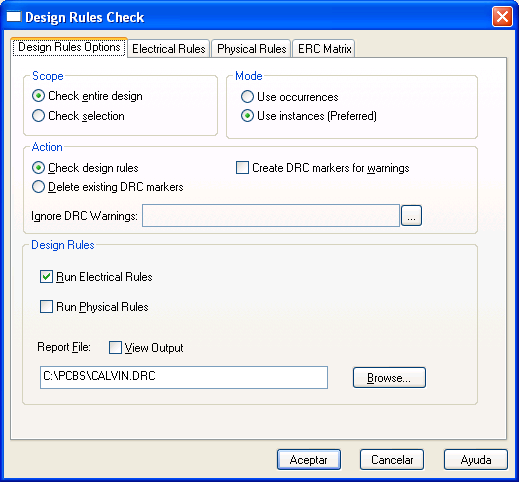
# How to compile an schematic

In order to compile a schematic follow these steps:

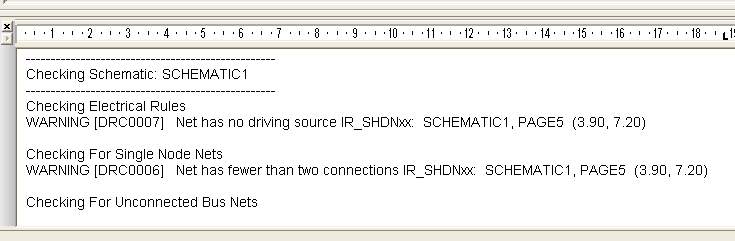
1. Select the main tab
2. Click on the main design option (\*.dsn field):
3. Click on “tools”\”Design Rules Check”. See following picture:



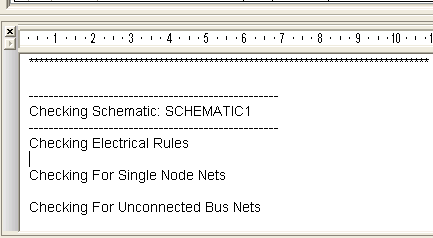
1. The following dialog box will appear. Click Ok to start the compilation.



1. The output of the compilation will be displayed at the bottom of the screen. Click of the bars to resize the output section. See following picture:



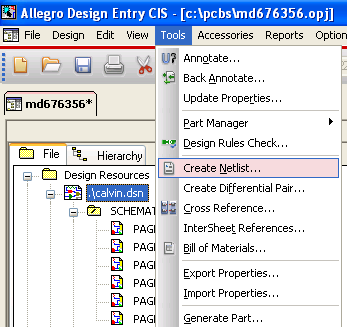
1. The schematic must be changed to address the list of errors and warnings displayed. Once all errors are fixed you should get the following output:



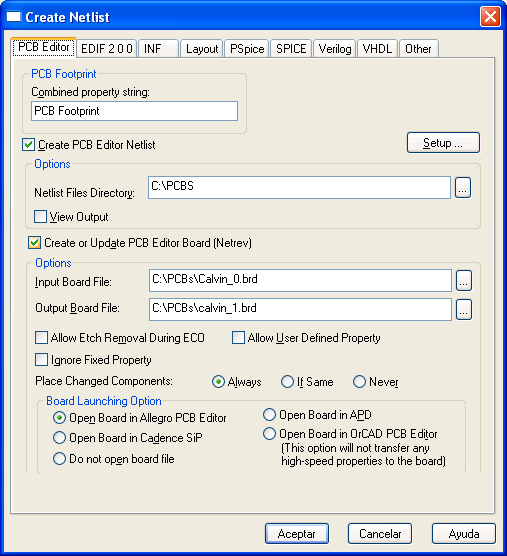
# How to create the netlist from schematic

In order to create the netlist follow these steps:

1. Select the main tab
2. Click on the main design option (\*.dsn field):
3. Click on “tools”\”Design Rules Check”. See following picture:

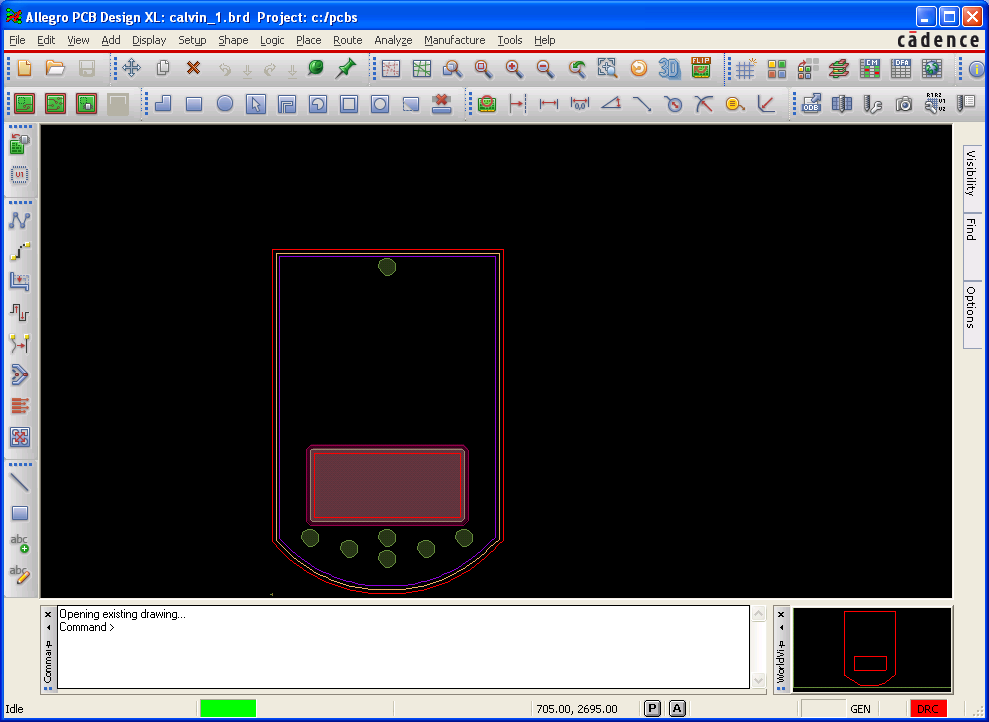


1. The following dialog box will appear. Click Ok to start the compilation.

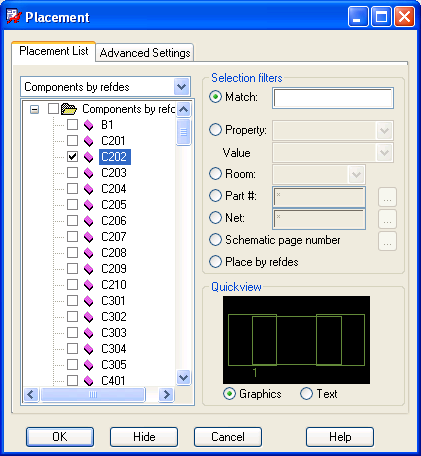


In this part it is important to introduce the **“Input Board File” and “Output Board File”**. These files are the board template. Where input board is taken as base and it will be updated to generate output board. Next time a netlist will be created the “output board file” is used as “input board file” and a new “output board file” is used.

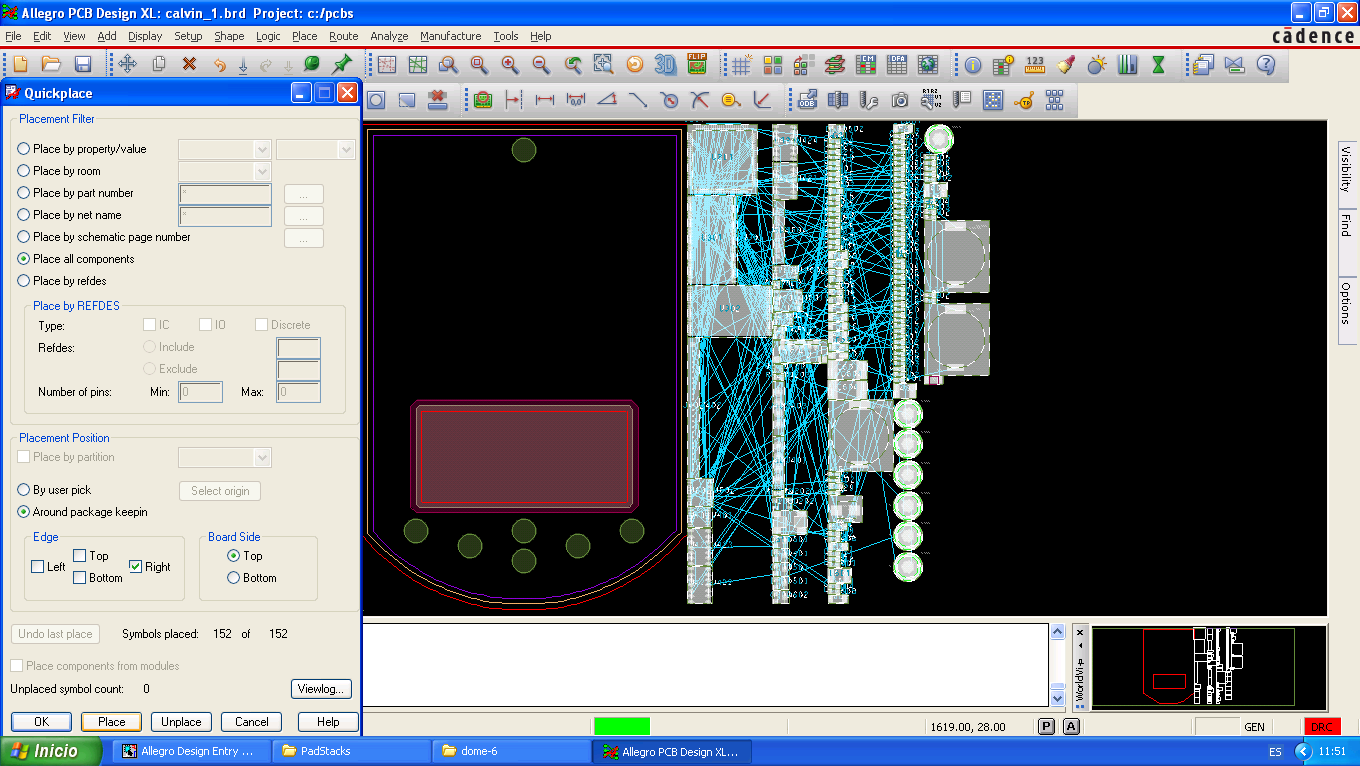
1. The output of the net list will be displayed at the bottom of the screen. Click of the bars to resize the output section. See at the end of this document the whole create netlist output.
2. Due to netlist links symbols, libraries and schematic, during the net list generation errors could be found anywhere. So in this process it will match the pins of the libraries with the footprint pins to ensure it really matches. For instance, if a library contains pins 1, 2 and 3 and footprint contains pins 1, 2, 4 it will display and error informing the pin 3 cannot be found and pin 4 is an extra pin. So need to update library or footprint in order to fix this problem and get no error in the net list creation.
3. At the end of the “create netlist” it will automatically open PCB editor, which will allow to do placement of the parts into the board. See following screen:



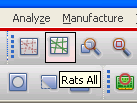
1. The final step is to place the parts through **“place”** menu. In this part we must ensure the parts of the schematic are correctly listed. There are two methods to place parts:
   1. **“manually”**  🡺 Individual or all parts are placed. The following dialog box shows this mode of placing.



* 1. **“quick place”** 🡺 Place all parts automatically. You can select the initial position where they will be placed. That is, top, bottom, left, right. Press **“Place”** button to place the parts. See following picture:

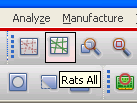


The lines displayed are named rats. You can enable and disable them through the following buttons:



# Rat nets in Layout

The lines displayed are named rat nets. You can enable and disable them through the following buttons:



Rat nets inform the closest pin target where a current pin is connected.

**Notes:**

* Rat nets can be connected to different other pins if moved to a different place or some other part is moved, this is due to there can be multiples pins connected to the same net, for instance power or GND, lot of pins have connection to them so if moved the rat nets will connect to the next pin containing this net.

# Setting Placement Constrains (DFA) in Layout

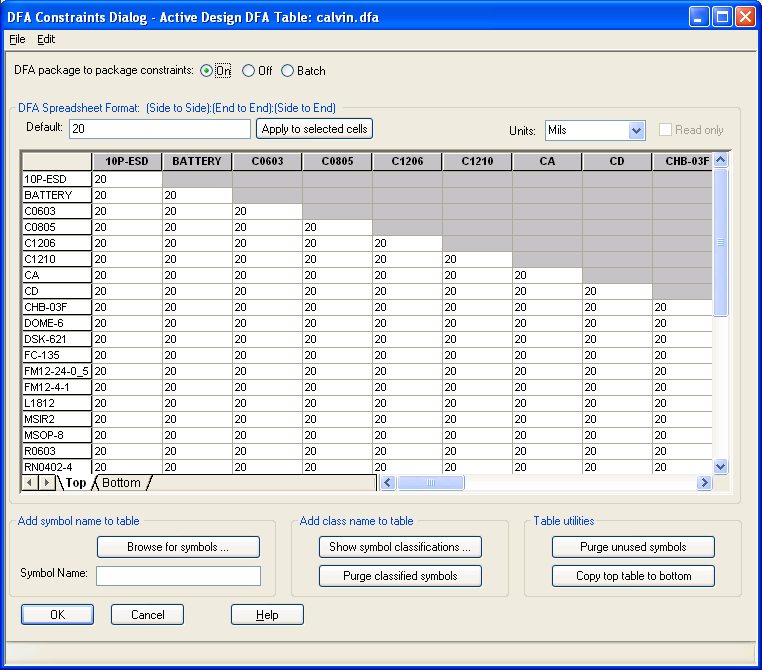
Before doing any placement the first step is to set the placement constrains in order to have proper information of **DRC** when breaking the placements constrains.

In order to set placement constrains follow this steps click on DFA button in the tool bar (). This can also be accessed through menu setup\Constrains\DFA Constrains Manager option.

**Note:**

Placement must be filled for **top** and **bottom** layers.

The See following picture shows DFA dialog box.



# Placements recommendation in Layout

This section provides a list of MUST and MUST NOT recommendations during placement.

The following are some recommendations:

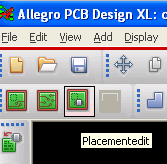
1. **Deactivate rat nets.** This will make easier the view. Rats net are automatically displayed for a part which is selected to be moved, so you will know where it is.
2. **Thing always in the routing**. In spite of DFA placement restrictions at placement time you should consider how many nets will pass between the elements. This will avoid rework for placement at routing time which is used to be expensive.
3. **Place the more important chip first**. Differential pairs first, buses second, and so on.
4. **Place the secondary related components close to the main chip**. This will make layout simple because most of the routing can be isolated.
5. **Place the chips in the same orientation.** This will reduce manufacturing costs due to in one single pass the machine will be able to place all parts.
6. **Send parts to bottom/top layers as needed through mirror function**. This is useful to release space in layers.

# Placement How to in Layout

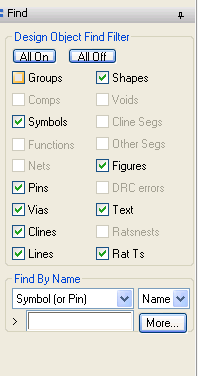
This section will provide a list of hints about how to do the placement.

**Moving parts from top/bottom layers.** This can be done as follow:

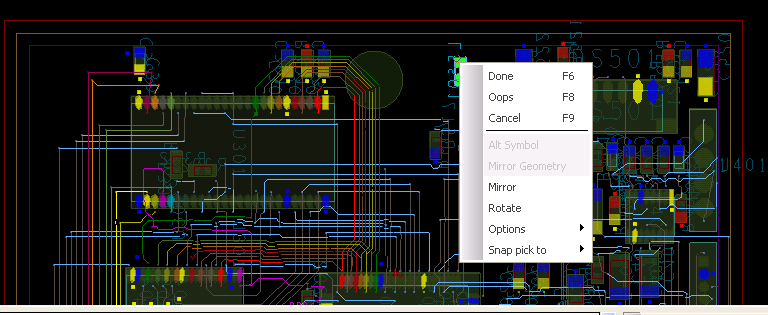
* Select placement edit:



* Turn **All On** in “Design Object Find Filter” in **find** tool box.



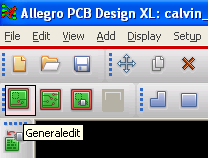
* Right Click on the part
* Click on **mirror** function.



**Rotating a part**. Follow same steps to mirroring and select **Rotate** instead of mirror.

**Removing a part**. Follow these steps:

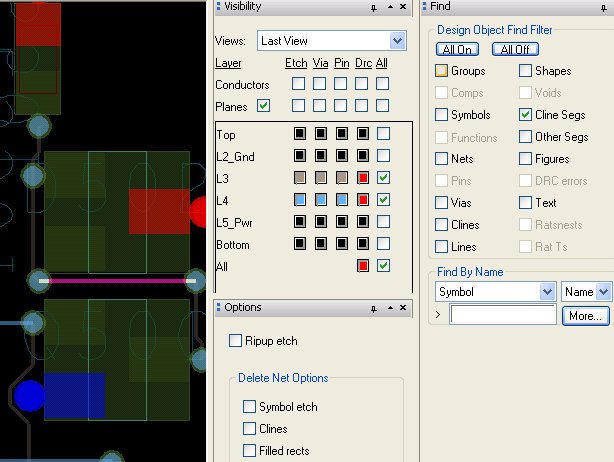
* Click on General Edit
* Click on  icon:



* On **find** tool box, select **what to delete**, For instance in this case we want to delete a segment of a **Cline** (part of a line) which is marked up with **magenta** color in the picture below.
* Click on the Cline Segment to be deleted.
* Right click and select **done**.

**Note:**

The Cline was already deleted in spite of it is still visible.

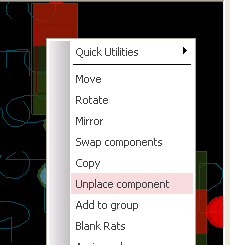
* 

**Placing a new part**. In order to place a part click on **Place** menu.

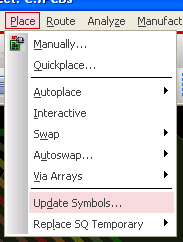
You have two options: **Place Manually** and **QuickPlace**. There is a dedicated section in this document to show how to do this.

**Update footprint changes in the board**. There are two methods:

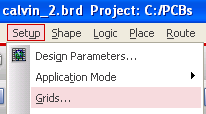
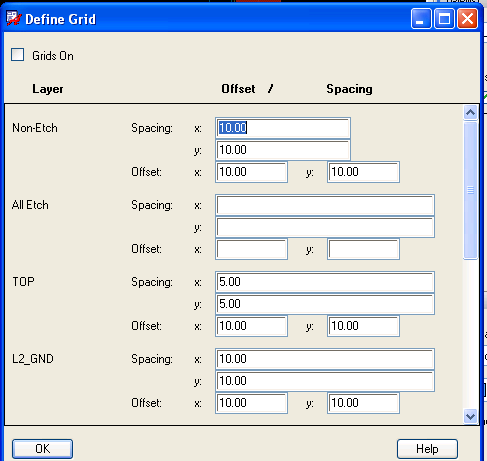
* **Updating an specific symbol.** This can be done by deleting the object and placing it again. This can be done by:
  + Selecting placement edit icon().
  + Right click on the part
  + Unplace component.



* **Updating all symbols**. This can be done through the **place** menu and **update symbols** option:



**Setting the grid**. This can be done through the **Setup** menu:

* 
* 

**Viewing board in 3D**. click on the 3D icon ().

**Turn around the whole board**. click on the FLIP icon ().

**Changing colors to the PINs and CLines**. click on the brush icon ().

**Deactivating/Activating elements/layers,etc**. click on Colors icon ().

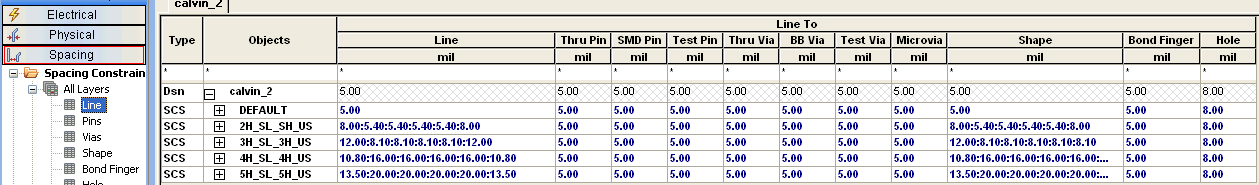
**Defining layout constrains**. Click on constrains icon (). This is a dedicated section to explain this in detail below.

# Constrains Manager in Layout

Once the parts are located the next step is to set the physical, electrical and spacing constrains. These are configured through Constrains manager ().

The following section will provide list of steps and how to about how to set up constrains.

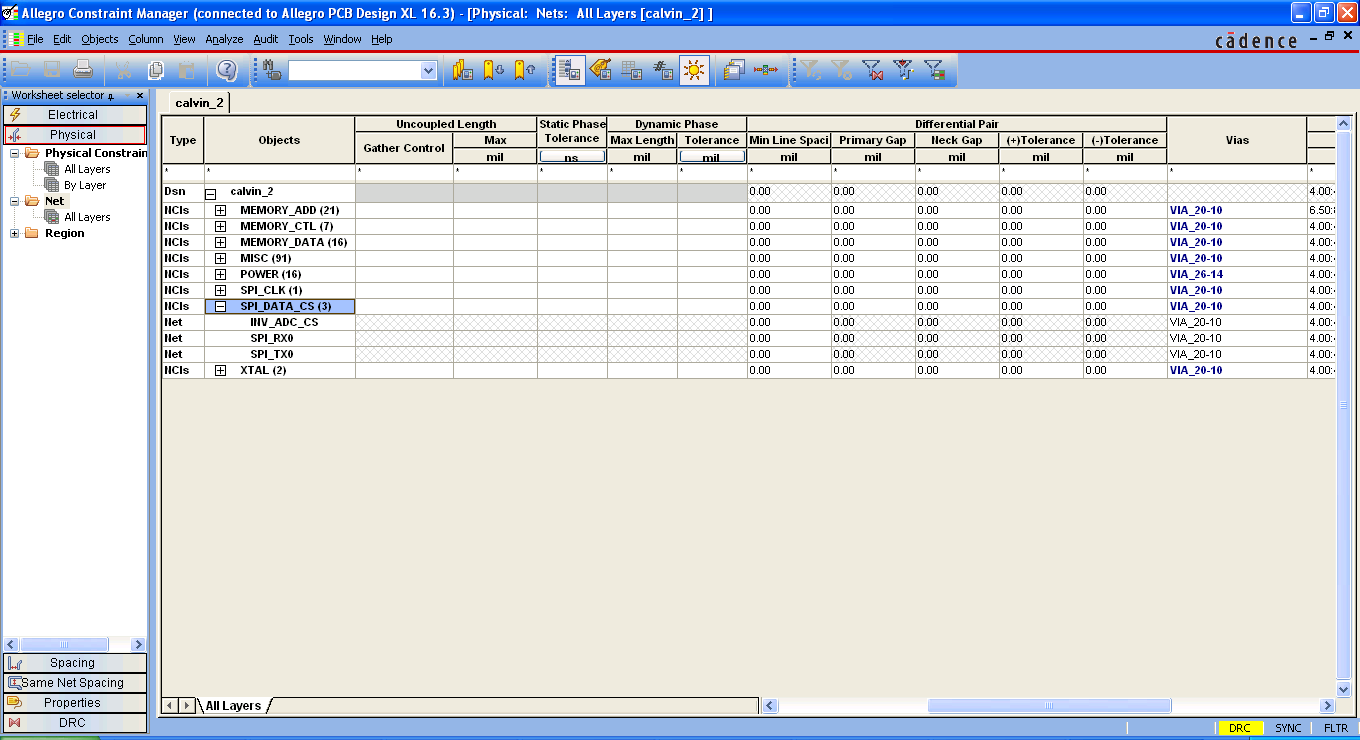
1. **Define the spacing constrains.** This can be done by clicking on **Spacing** tab and selecting **spacing constrains**. See picture below.



In order to define a new spacing constrain:

* do **mouse right click** and select **create\spacing**.
* Name the spacing constrain
* Update Line, shape, via, etc. constrains.

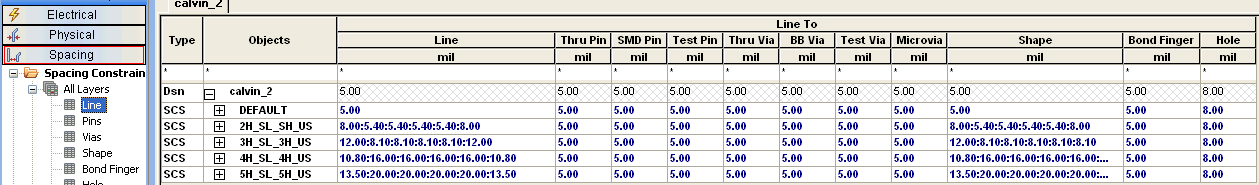
1. **Define the classes.** This can be done by clicking on **Spacing** tab and selecting **nets**. See picture below.



In order to define a class constrain:

* do **mouse right click** and select **create\class**.
* Name the class
* Select the nets belonging to the class.
* See previous picture as an example.

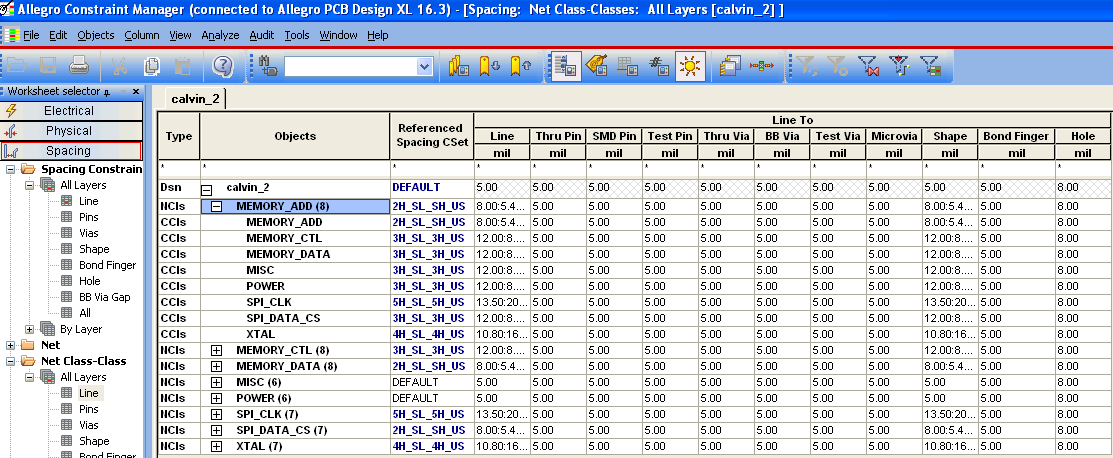
1. **Define the vias.** Go to the Vias column and select the name of the vias (they must be located in the padstack path).
2. **Define the net class CSet Space constrains.** This can be done by clicking on **Spacing** tab and selecting **spacing constrains**. See picture below.



In order to define a new spacing constrain:

* do **mouse right click** and select **create\spacing**.
* Name the spacing constrain
* Update Line, shape, via, etc. constrains.

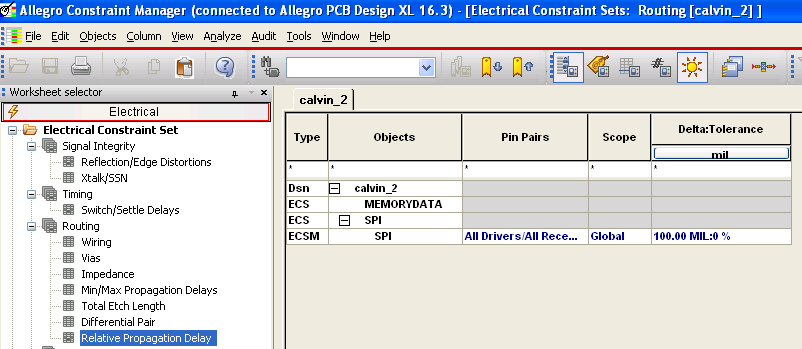
1. **Define the net class-class constrains.** This can be done by clicking on **Spacing** tab and selecting **net class-class constrains**. See picture below.



In order to define a new spacing constrain:

* Do **mouse right click** and select **create\class-class**.
* In the left size select the net classes, in the right size select the net classes which will be constrains against to.
* Update Line, shape, via, etc. constrains.

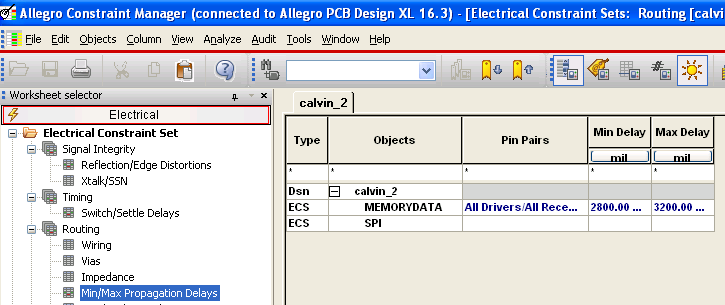
1. **define the electrical constrains for propagation delay.** This can be done by clicking on **Electrical Constrain Set** tab and selecting **Relative Prograpation Delay**. See picture below.



In order to define a new spacing constrain:

* Do **mouse right click** and select **create\Electrical CSet**.
* Name it as SPI with 100 mils and 0%

1. **define the electrical constrains for propagation delay.** This can be done by clicking on **Electrical Constrain Set** tab and selecting **Min/Max Propagation Delays**. See picture below.



In order to define a new spacing constrain:

* Do **mouse right click** and select **create\Electrical CSet**.
* Name it as MEMORYDATA with 2800 mils and 3200 mils for min and max delays

1. At this point all routing constrains were made. Close the Constrain manager and save the board in the PCB Editor.

# Issues found

All issues found were already addressed in the explanations of topics above.

# Conclusions

The main issues found where related the allegro tool which is not aligned to the current available tools making this tool hard to understand….

After spending lot of hours in this tool I finally understood lot of stuff but I was never be able to dominate the footprints generation at this point.

Allegro is a very powerful but the usage will cause this tool to be absolute and no longer be used due to their complexity in user interface and management.

I definitely would explore for other tools when in the future want to create a board.